Development of Power Quality event using Diode Clamped Multilevel Inverter in conjunction with AANF

Dr.B.Gopinath,M.E.,Ph.D.,

Associate Professor/Dept of EEE

Vivekanandha College of Engineering for Women

Elayampalayam,Tiruchengode

[gopivce@gmail.com](mailto:gopivce@gmail.com)

V.Karthika,

PG student, Dept of EEE

M.Kalyanasundaram,M.E.,(Ph.D)

Assistant professor, Dept of EEE

Vivekanandha College of Engineering for Women

Elayampalayam,Tiruchengode

[mkalyanasundharam79@gmail.com](mailto:mkalyanasundharam79@gmail.com)

M.Pradeepa

PG Student,Dept of EEE

Vivekanandha College of Engineering for Women Vivekanandha college of Engineering for Women

Elayampalayam,Tiruchengode Elayampalayam,Tiruchengode

[karthimepse@gmail.com](mailto:karthimepse@gmail.com) [mpradee.226@gmail.com](mailto:mpradee.226@gmail.com)

*Abstract*—T**his paper presents the performance of Power Quality (PQ) which is improved by using diode clamped multilevel inverter. Due to synchronization the grid interfaced performance of DG systems affected by PQ events such as, balanced and unbalanced voltage sag/swell, frequency shift, phase jump and harmonic distortions. In this proposed paper the five level inverter is used to reduce harmonics. The droop control technique is also used to produce PWM. Capacitors are also used to eliminate unwanted noises that occur in the voltage side. Here an Amplitude Adaptive Notch Filter (AANF) is used for detection of utility voltage, phase angle due to its adjustable accuracy and also estimate frequency and its amplitude. The proposed control technique in integrating the Dg system for PQ events to the utility grid is done using MATLAB simulations.**

Keywords—Diode clamped inverter, Droop controller, Grid interfaced, DG systems, power Quality improvement.

# I. Introduction

**E**lectric utilities and end users of electric power are becoming increasingly concerned about meeting the growing energy demand. Seventy five percent of total global energy demand is supplied by the burning of fossil fuels. Since the past decade, there has been an enormous interest in many countries on renewable energy for power generation. Renewable energy source (RES) integrated at distribution level is termed as Distributed Generation (DG) [1]. The utility is concerned due to the high penetration level of intermittent RES in distribution systems as it may pose a threat to network in terms of stability, voltage regulation and Power-Quality (PQ) issues. Therefore, the DG systems are required to comply with strict technical and regulatory frameworks to ensure safe, reliable and efficient operation of overall network.

All the control techniques for interconnection of DG units to utility grid are developed to achieve specific objectives. The three phase voltage source inverter (VSI) which controls the injected active power flow from DG units to the utility grid [2]. In addition, it will compensate load reactive power demand and also nonlinear load harmonic current under changing load conditions. In this paper it has a combination of an adaptive notch filter (ANF) based synchronization technique developed.

Interconnection of DG systems based on renewable energy sources such as, solar photovoltaic (PV) systems, wind farms, mini-hydro power generation units, fuel cells, etc. are gaining more popularity in various countries all over the world. This novel concept of interconnection of DG systems plays an important role in maintaining reliability and stability of the utility grid by fulfilling today’s increasing demand of electricity [4]. Furthermore, one of the most significant issues for DGS is the control methods in different operation modes. Many papers have been presented for the controls of islanded mode and grid-connected mode. Another significant issue is grid synchronization. The grid synchronization method has been elaborately discussed for single grid-connected converters. However, it is not often explored for multi-converter oriented systems or droop controlled DGS.

With the gradual failure of conventional energy sources and the increase of environment pollution, countries around the world began to focus on eco-friendly, efficient and flexible power generations-DG. The rapid development of DG generations has provided a lot of clean and efficient energy for the community, but has also brought great challenges to the existing power system [3]. In order to reduce the adverse impact on the existing distribution network bought by DG while give play to its auxiliary function, which is the effective use of renewable energy, micro-grid, as an important form of DG has gained attention and promotion from many countries around the world. Micro-grid is an individually controllable system composed of load and distributed power supply, and it provides electricity and heat to local load.

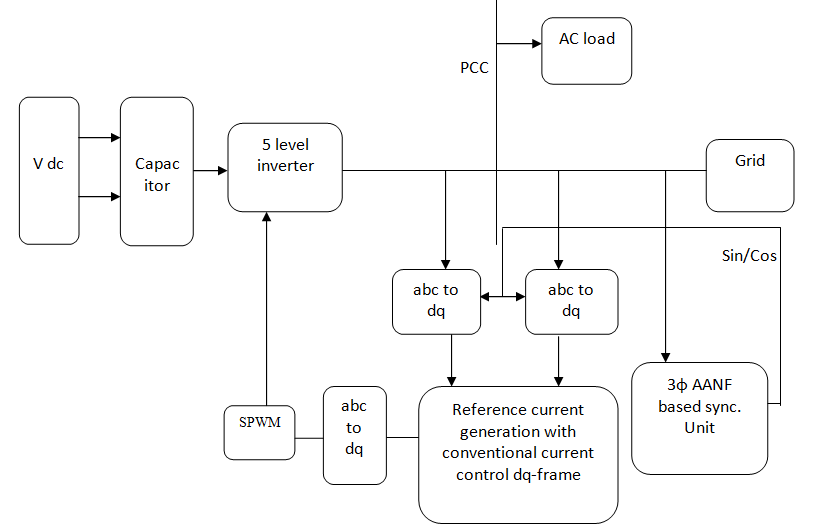
The three phase voltages and currents at the point of common coupling are measured and this is given as input to the controller and also to the DC link regulator. Then these three phase voltages and currents are converted into stationary α-β values. Sequence extractor then transforms these values of voltages in the form symmetric components. To maintain the power flow into the grid the DC link voltage has been controlled by the DC link controller by using active power reference P.

This paper also presents an amplitude adaptive notch filtering (AANF). It offers a high degree of immunity and insensitivity to power system disturbances that exist in the grid signal. Compared with SOGI-FLL, the immediate difference is

Adaptive filter. The second order generalized integrator is used and adaptive filter is employed in the structure. The AANF can estimate the frequency, amplitude and other useful information of a random grid signal. Its performance of frequency and amplitude estimation is better than the traditional ANF when the grid signal is of variable amplitude.

# II. PROPOSED SYSTEM

Fig 1.shows the block diagram of the proposed system. In this paper the levels of the inverter are increased which is used to reduce harmonics. It consist of droop controller, transformers, diode clamped multilevel inverter, Grid, capacitors are used for the better performance.



## Fig. 1 Block Diagram for Proposed System

## Multilevel inverter

The term multilevel starts with the three-level inverter introduced by Nabae []. By increasing the number of levels in the inverter, the output voltages have more steps generating a staircase waveform, which has a reduced harmonic distortion. However, a high number of levels increases the control complexity and introduces voltage imbalance problems.

The most attractive features of multilevel inverters are as follows.

1) They can generate output voltages with extremely low

distortion and lower .

2) They draw input current with very low distortion.

3) They generate smaller common-mode (CM) voltage, thus reducing the stress in the motor bearings. In addition, using sophisticated modulation methods, CM voltages can be eliminated.

4) They can operate with a lower switching frequency.

The basic three types of multilevel topologies used are:

* Diode clamped multilevel inverters
* Flying capacitors multilevel inverter or Capacitor clamped multilevel inverter
* Cascaded inverter with separate dc source.

## Diode Clamped Multilevel Inverter

The first invention in multilevel converters was the so-called neutral point clamped inverter. It was initially proposed as a three level inverter. It has been shown that the principle of diode clamping can extended to any level.

The diode-clamped type inverter is used for experimentations in this project. Such inverter employs the technique of proportional stepping harmonic elimination type to control switching equipment in the circuit for providing appropriated waveform and increasing the efficiency at high loading. The diode-clamp and modulate principle are implemented to control the output waveform approaching to the sine-wave as close as possible.

The most commonly used multilevel topology is the diode clamped inverter, in which the diode is used as the clamping device to clamp the dc bus voltage so as to achieve steps in the output voltage. Thus, the main concept of this inverter is to use diodes to limit the power devices voltage stress. The voltage over each capacitor and each switch is *Vdc*. An *m* level inverter needs (*m*-1) voltage sources, 2(*m*-1) switching devices and 2 (*m*-2) diodes. By increasing the number of voltage levels the quality of the output voltage is improved and the voltage waveform becomes closer to sinusoidal waveform. The Fig.2 shows the five level diode clamped inverter.

The main advantages and disadvantages of this topology are:

Advantages:

* High efficiency for the fundamental switching frequency.
* The capacitors can be pre-charged together at the desired voltage level.
* The capacitance requirement of the inverter is minimized due to all phases sharing a common DC link.

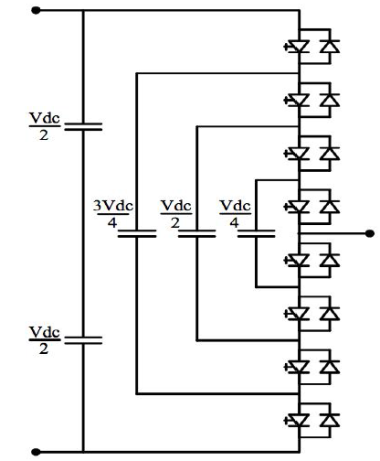


Fig. 2 Five level DCMI structure

Disadvantages:

* Packaging for inverters with a high number of levels could be a problem due to the quadratically relation between the number of diodes and the numbers of levels.
* Intermediate DC levels tend to be uneven without the appropriate control making the real power transmission a problem.
* Uneven rating in the diodes needed for the converter.

Some of the applications using Multilevel Diode

Clamped converters are:

* An interface between High voltage DC transmission line and AC transmission line.
* High power medium voltage variable speed drives.
* Static VAR compensation.

The 5 level diode clamped multilevel inverter uses switches, diodes. a single capacitor is used ,so output voltage is half of the input dc.

The steps to synthesis the five level phase a output voltage in this work are as follows

1. For phase a output voltage of Van=0, two upper switches Sa3, Sa4 and two lower switches Sa1‟ and Sa2‟ are turned on.

2. For an output voltage of Van=Vdc/4, three upper switches Sa2, Sa3, Sa4 and one lower switch Sa1‟ are turned on.

3. For an output voltage of Van=Vdc/2, all upper switches Sa1 through Sa4 are turned on.

4. To obtain the output voltage of Van= -Vdc/4, upper switch Sa4 and three lower switches Sa1‟, Sa2‟ and Sa3‟ are turned on.

5. For an output voltage of Van = -Vdc/2, all lower switches Sa1‟ through Sa4‟ are turned on.

**TABLE I: Switching Scheme for one phase of three phase five Level DCMLI**

|  |  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- | --- |
| **S1** | **S2** | **S3** | **S4** | **S1’** | **S2’** | **S3’** | **S4’** | **Van** |
| 1 | 1 | 1 | 1 | 0 | 0 | 0 | 0 | Vdc/2 |
| 0 | 1 | 1 | 1 | 1 | 0 | 0 | 0 | Vdc/4 |
| 0 | 0 | 1 | 1 | 1 | 1 | 0 | 0 | 0 |
| 0 | 0 | 0 | 1 | 1 | 1 | 1 | 0 | **-**Vdc/4 |
| 0 | 0 | 0 | 0 | 1 | 1 | 1 | 1 | **-**Vdc/2 |

The switches are arranged into 4 pairs (Sa1, Sa1‟), (Sa2, Sa2‟), (Sa3, Sa3‟), (Sa4, Sa4‟). If one switch of the pair is turned on, the complementary switch of the same pair must be off. Four switches are triggered at any point of time to select the desired level in the five level DCMLI. The phase a output voltage Van has five states: Vdc/2, Vdc/4, 0, - Vdc/4 and - Vdc/2. The gate signals for the chosen five level DCMLI are developed using MATLAB-SIMULINK. The gate signal generator model developed is tested for various values of modulation index. The results of the simulation study are presented in this work in the form of the PWM outputs of the chosen multilevel inverter.

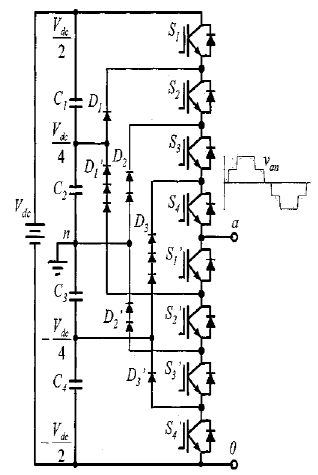


Fig. 3 Five level Diode-clamped multilevel inverter circuit

Topology

1. *ABC to DQ Frame*

The three-phase current is the AC current of a three-phase circuit, while the d, q currents are the direct current and quad current in the flux, torque (d, q) rotating reference frame.

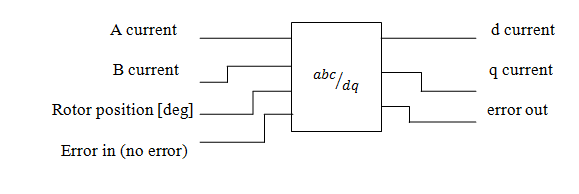


Fig. 4 Structure of abc to dq frame

Where, **a current** - specifies the a current, in amperes, of

the three-phase current.

**b current**- specifies the b current, in amperes, of

the three-phase current.

**rotor position-**specifies the rotor position, in degrees, of the electric motor.

**error in-**describes error conditions that occur

before this node runs.

**d current-**returns the direct current, in amperes,

from the Clarke and Park transform.

**q current** returns the quad current, in

amperes, from the Clarke and Park transform.

**error out**  contains error information. This

output provides standard error out functionality.

1. *ABC to DQ transform details*

This VI assumes that *Ia+Ib+Ic*=0, where *Ia* is the value of the a current, *Ib* is the value of the b current, and *Ic* is the value of the c current of the three-phase current. The following equations convert three-phase current to direct and quad current:

(1)

(2)

Where is the d or direct current;is the q or quad current; *θ* is the rotor position in radians.The values of and are also derived from the following equations:

(3)

(4)

Where,

and

1. *AANF*

In synchronization scheme, the dc component which may be an intrinsic component of the input signal should be considered. The technique to deal with this problem can be found. In addition to the methods mentioned above, adaptive notch filter (ANF) is also an important tool. In order to improve the performance of the ANF, its structure is modified through optimizing the dynamic equation. In addition to the frequency, the ANF can output very useful signal information such as amplitude, the fundamental component and its 90 degree phase-shift. The ANF has been used in various applications. The ANF-based scheme is simpler than the PLL-based approaches, and overcomes some shortcomings of the PLL systems. However, it ignores an key factor that the amplitude of the signal influences the performance of estimation.

An amplitude adaptive notch filtering (AANF), offers a high degree of immunity and insensitivity to power system disturbances that exist in the grid signal. Compared with SOGI-FLL, the immediate difference is adaptive filter. The second order generalized integrator is used and adaptive filter is employed. The AANF can estimate the frequency, amplitude and other useful information of a random grid signal. Its performance of frequency and amplitude estimation is better than the traditional ANF when the grid signal is of a variable amplitude.

1. *Structure of the AANF*

Fig.5 shows the detail structure of the AANF.

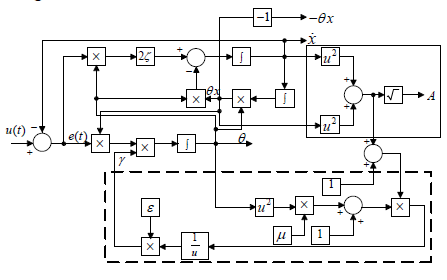


Fig.5 Detail structure of the AANF.

The power of the AANF is that it outputs useful signal information such as the fundamental component, its 90 degree phase-shift, amplitude and frequency. The difference of the proposed AANF with respect to conventional ANF is the adaptation to the input signal amplitude which is surrounded by dotted line. According to the unique periodic orbit, andare the fundamental component and its 90-degree phase shift, respectively. The amplitude of the input signal is easily calculated by some simple operations that are surrounded by solid line. ω is the fundamental frequency of the input signal.

*g. Its Problem*

*Problem definition*

In grid-connected converters, the input signal to the synchronization tool is in the form defined in equation 5

(5)

The nonzero amplitudes, *Ai* , *i* =1,2,……, *n* , the nonzero frequencies, , *i* =1,2……, *n* , and the phases , *i* =1,2……, *n* , are typically unknown parameters. Estimating unknown parameters, especially when the grid voltage is not standard, is a necessary task in many applications.

*Anf Dynamic And Structure*

A globally convergent adaptive notch filter (ANF) is proposed to estimate online the unknown frequency, the dynamic equation is:

(6)

Where , *N* , are real positive parameters. *u*(*t*) is the input signal. In (3.8), θ represents the estimated frequency, and ζ and γ are damping ratio and adaptation gain, respectively. ζ determines the “depth of the notch” , and γ determines the “adaptation speed”.

## III. SIMULATION RESULT AND DISCUSSION

To verify the performance, the complete five-level diode clamped inverter DG systems model described in the previous section is simulated using power system toolboxes in the MATLAB environment. The DG system simulation paramneters are tabulated in Table 1.

TABLE II:THE DG SYSTEM PARAMETERS

|  |  |  |
| --- | --- | --- |
| S.NO | PARAMETER | VALUE |
| 1 | System frequency(f) | 50HZ |
| 2 | Switching frequency(fsw) | 3150HZ |
| 3 | DC link voltage | 750V |
| 4 | Nominal grid voltage(VG) | 400V(L-L) |
| 5 | Coupling Inductance(Lc) | 4.9mH |

The simulation for this paper characterized as SI control strategy, Droop control, PWM units, power calculation, subsystem, virtual impedance loop.

The overall simulation is done using MATLAB.This simulation is validated and gives the performance improvement and makes the system stable is illustrated in Fig. 6.

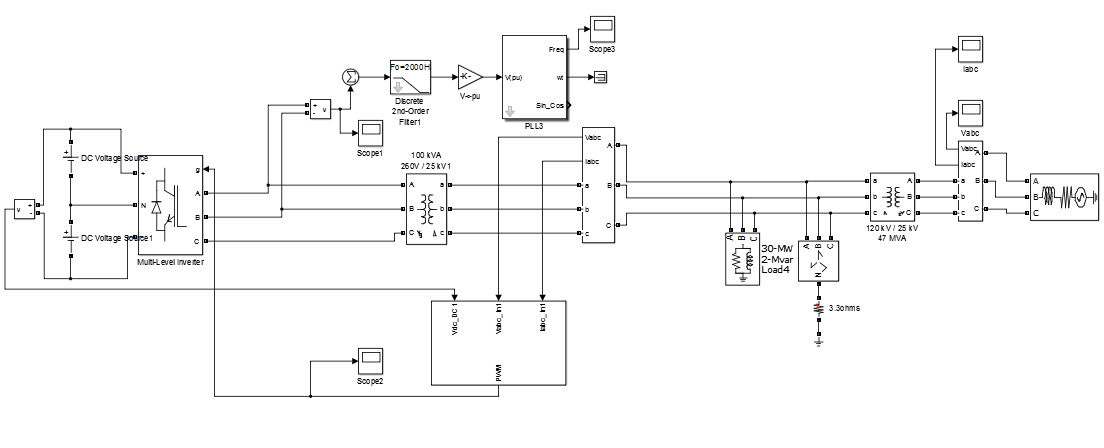


Fig.6 Simulink Implementation of the proposed system

The below waveform shows about the frequency that occurs in the system which is illustrated in Fig.7.It shows how much the time taken to make the system stable and also it is clear after sometime then the system becomes stable.

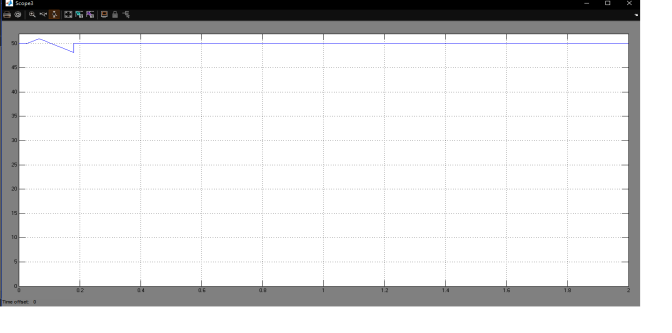


Fig.7 Frequency waveform

The three phase diode clamped five level inverter is modeled in SIMULINK using power system block set.Simulations are performed for different values of ma ranging from 0.6 to 1 and the corresponding % THD are measured using the FFT block and their values.It is observed that the strategy produces significant 33rd.35th and 37th harmonic spectrum,speed and torque characteristics are done with above strategies but only one sample of ma=0.8 which is shown in Fig. 8.

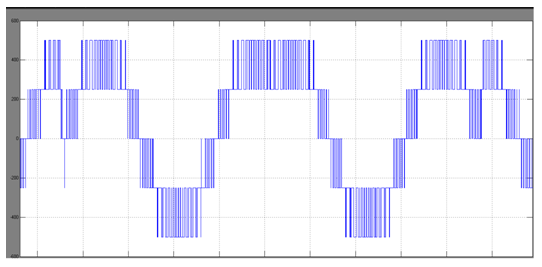


Fig.8 voltage waveform of inverter

The Figure 9 & 10 shows the current and voltage waveform of grid.using a grid system in this design also allows for that sense of uniformity and familiarity while it may work for some sites to have vastly different page designs,for many,it will not be the case and it will want to have a uniform and more structured feel to the main layout.

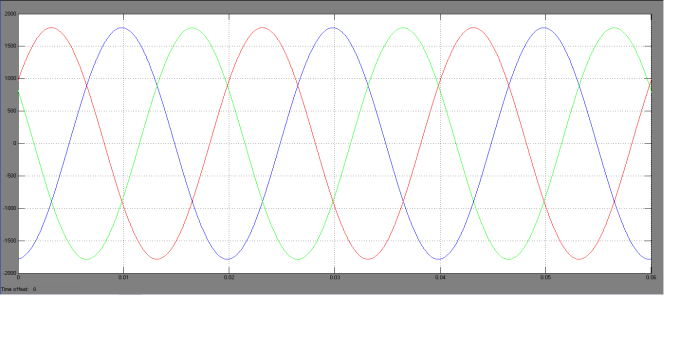


Fig. 9 current waveform of grid

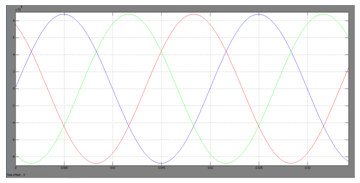


Fig.10 Voltage waveform of grid

When the signal is high, we call this “on time”. To describe the amount of “on time” , we use the concept of duty cycle. Duty cycle is measured in percentage. The percentage duty cycle specifically describes the percentage of time a digital signal is on over an interval or period of time shown in figure 11. This period is the inverse of the frequency of the waveform. If a digital signal spends half of the time on and the other half off, we would say the digital signal has a duty cycle of 50% and resembles an ideal square wave. If the percentage is higher the digital signal spends more time in the high state than the low state and vice versa if the duty cycle is less than 50%. 100% duty cycle would be the same as setting the voltage to 5 Volts (high).

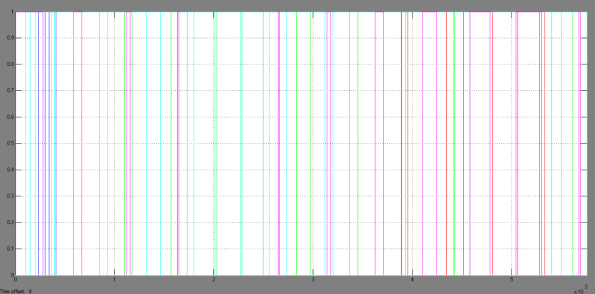


Fig 11 waveform of PWM signal

IV. CONCLUSION

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In this paper the using of five level inverter reduced the harmonics level with the help of voltage source inverter. Capacitors are used to filter out the noises that occur in the DC sources. The VSI converts DC to AC where the grid normally generates AC. Robust behavior of three phase AANF enhances the control performance of the DG system. In order to avoid that three AANF based dq-current control technique for five level NPC grid interfaced inverter DG system is used for filtering the occurred harmonics. This control circuit operates DG system I UPF mode by injecting only active power into the utility grid. The using of droop controller produced the PWM units. Therefore the various simulations shows the reduction of harmonics and improving the performance of power quality.

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